Abstract

10

A ferroelectric memory device including an extended memory unit features a cell array block, a data bus unit, an input/output circuit unit, an extended memory unit and extended memory controller. The cell array block includes a main bitline and a plurlaity of sub bitlines. The main bitline is connected between a main bitline pullup controller and a column selection controller, and each sub bitline is connected to the main bitline and a unit The data bus unit is connected to the column cell. selection controller. The input/output circuit unit includes a sense amplifier array connected to the data bus The extended memory unit shares the main bitline unit. included in the cell array block and includes a plurality of cell blocks. The extended memory controller controls the extended memory unit in response to an external control signal.